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(54) Structure and method for fabricating of a field emission device

(57) The invention generally relates to the technical field of devices using the effect to emit electrons out of a solid into vacuum due to high electric field strength. Such devices are usually called field emission devices. The invention relates more specifically to the structure of a field emission device and to methods of fabricating a field emission device.

The inventive structure of a field emission device comprises a tip 1 for emitting electrons, said tip 1 has a body 2 of a first material, said body forms a series resistor, said tip is centered in relation to a gate aperture 3 which in particular is a circular gate aperture formed by an electrode 4, wherein said tip 1 projects above the surface of said electrode 4 forming the gate aperture 3.

The inventive method for fabricating a field emission device allows the critical dimensions of the tips and the gate electrode to be independently controllable and thus offers a large process window and an easy manufacturability. The range of threshold voltages at which devices emit which have been processed according to the inventive methods is very small and thus offers high multiplexibility.

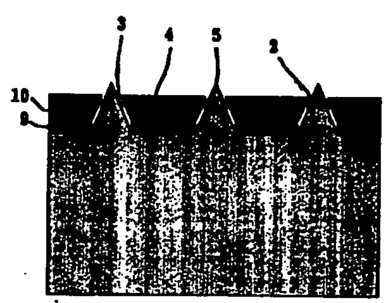

FIG. 1F

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Description

Technical Field

The present invention relates to the technical field of devices using the effect to emit electrons out of a solid into vacuum due to high electric field strength. Such devices are usually called "field emission devices". The invention relates to the structure of a field emission device, to the method of fabricating a field emission device, and, more specifically, to the use of a multitude of field emission devices in the technical field of flat panel displays.

Background Art

Field emission devices can be used to replace conventional thermal emission devices as electron sources for e.g. scanning electron microscopes, high performance and high frequency vacuum tubes, and, more general, for vacuum microelectronic devices.

In recent years there has been a growing interest in using miniaturized field emission devices in the technical field of flat panel displays. A miniaturized device which uses a multitude of tips or microtips for electron emission simultaneously and which achieves high electric field strengths, by applying fairly low voltages due to tip-to-electrode distances in the micron range was firstly proposed by C.A. Spindt in Journal of Applied Physics, Vol. 39 (1968), No. 7, pages 3504 - 3505. Several publications by the same author and by others followed over the last twenty years. A comprehensive review is given in IEEE Transactions on Electron Devices, Vol. 38 (1991), No. 10, pages 2289-2400.

A typical field emission device comprises a conductive tip placed on a conductive electrode which usually forms the cathode electrode. The tip end is surrounded by a gate electrode. An appropriate voltage is applied between the cathode and the gate electrode to emit electrons into the vacuum. For the application of these field emission devices in the technical field of flat panel displays the tip and gate arrangement is encapsulated by an upper and lower glass plate.
The upper glass plate contains the anode electrode and a phosphorous layer. An applied voltage between the cathode and the anode electrode accelerates the electrons emitted by the tips towards the phosphorous layer which emits visible light as usable in a display device. Gate and cathode electrodes are typically arranged in orthogonal stripes which allows matrix addressing of the electron emitting tips. Usually, an array of typically 1,000 tips is forming one pixel.

One major problem of the application of field emission devices as light emitting sources in flat panel displays is the non-uniformity in the emission characteristics of the multitude of tips. For a field emission device it is very important that the range of threshold voltages, at which individual tips emit, is as small as possible. This allows for a better multiplexing behaviour. The reliability of tip emission depends on several factors like applied voltage, cleanliness of the tips, vacuum quality, geometry, materials, etc. The field emission is extremely sensitive to the above cited factors. Despite the fact, the about 1,000 tips were electrically driven in parallel and should form one pixel, it was not able to achieve stable and uniformly illuminated pixels. Typically a few of the tips operating at a high current level bursted and caused short circuits between the cathode and the gate electrode. As a consequence, this short circuit disables a complete cathode and gate electrode stripe.

In A. Ghis et al: "Field Vacuum Devices: Fluorescent Microtip Displays", IEEE Transactions on Electron Devices, Vol. 38 (1991), No. 10, pages 2320 - 2322, which can be regarded as the nearest prior art document according to the structure of a field emission device of the present invention, a polysilicon resistive layer underlying a multitude of tips was introduced by which the current flowing through the tips was limited. An electron emitting tip which is connected via a resistive layer to a conductive layer which is the cathode electrode.
This arrangement is built on a first glass substrate. The third conductive layer, which is the gate electrode, is separated from the first conductive layer by a dielectric layer. The first conductive layer acts as a series resistant layer for each tip.

Each pixel was divided in 50 groups of tips, each group consists of 36 tips. Each tip within a group is connected via a common polysilicon resistive layer to the cathode electrode which is meshed. Therefore, there is no cathode electrode metallization directly underneath the tips. Therefore, in case of a short circuit between one tip and its respective gate electrode the whole pixel (made of 50 groups) will not be affected. However, it is still disadvantageous that in case of a failure of one tip the respective complete group of tips will fail. It is also disadvantageous that there is a considerable voltage drop within one group of tips caused by the various distances between individual tips and the cathode electrode which leads to different values of the series resistance for each individual tip. This voltage drop requires a considerably higher driving voltage and also power consumption and results in less tip emission current.
Furthermore, the voltage drop causes a non-uniform emission within one group of tips and therefore causes a non-uniformity in pixel brightness.

The method for fabricating of field emission devices has a significant influence on the performance of field emission devices in each of the applications of field emission devices mentioned above. In T. Asano: "Simulation of Geometrical Change Effects on Electrical Characteristics of Micrometer-Size Vacuum Triode with Field Emitters", IEEE Transactions on Electron Devices, Vol. 38 (1991), No. 10, pages 2392 - 2394, a simulation of the change in electrical characteristic of a field emission device due to changes in physical dimensions has been

described. A major result of this simulation is that the deviation of the gate opening size more strongly effects the field strength near the tip than a misalignment of tip and gate aperture. Furthermore, the simulation shows that this effect is more pronounced when the gate voltage is low. These results show the significance of a well controlled geometry of the field emission device and therefore the impact of an appropriate fabrication method.

In US patent no. 4,168,213 (Hoebrechts), US patent no. 5,126,287 (Jones) methods for fabricating field emission devices are described that use partially self aligned processing techniques. In the US patent no. 5,141,459 (Zimmerman) a fabricating process for field emission cathodes using conformal layer deposition on a sacrificial dielectric layer is described. Since the diameter of the gate electrode aperture is a significant parameter for the emission efficiency, and therefore should be minimized to achieve high emission efficiency, it is disadvantageous from the described fabrication process that a small gate aperture diameter can only be achieved by a high resolution lithographic, depositing, and etching technology, e.g. to realize submicron gate aperture diameter requires submicron lithographic, depositing, and etching technology. These high technology requirements are further more disadvantageous for the application of field emission devices in the technical field of flat panel displays with their typically large substrate dimensions.

The unpublished application EP-A-94113601 discloses a structure of a field emission device which comprises an individual series resistor for each electron emitting tip, wherein the series resistor is formed by the tip itself. The tip comprises a body of a first material with high resistivity and an at least partial coating of a second material with low work function, wherein the body of the first material forms the series resistor and the coating of the second material provides for electron emission. The method for fabricating a field emission device uses depositing and sacrificial layer etch back techniques to provide easy and precise control of tip height and shape and also easy and precise control of the lateral tip-to-gate distance and geometry. The method requires a bonding process for bonding a first substrate to a second substrate. This bonding step imposes objectives onto the manufacturability of the structure which might limit the size of the flat panel display substrates.

Some of the prior art methods for fabricating field emission devices are using certain lithographic, depositing, and etching processes as normally used in the technical field of semiconductor process technology. In S.M. Sze: "VLSI Technology", McGraw-Hill, New York, 1988, theoretical and practical aspects of the VLSI (Very Large Scale Integration) technology, as the present standard for semiconductor process technology are described.

Objects of the Invention

It is an object of the invention to provide a field emission device with reliable and reproducible performance concerning the emission efficiency even in the case of geometrical variation of the tip-gate electrode arrangement. For the application of field emission devices in the technical field of flat panel displays using a multitude of tips forming one of a multitude of pixels it is another object of the invention to provide an electron emission device with a high uniformity in emission efficiency from tip to tip.

Concerning the method for fabricating a field emission device it is an object of the invention to provide a method for fabricating with relaxed process requirements for a given gate aperture diameter and a method for fabricating which allows the reliable control of the lateral and vertical tip to gate distance.

Summary of the Invention

The objects of the invention are fulfilled by the characteristics stated in independent claims 1 and 6. Further arrangements of the invention are disclosed in the according dependent claims.

The invention as described in independent claim 1 eliminates the disadvantages previously described for the prior art. A field emission device with a series resistor formed by the tip itself can be directly connected to the supply electrode, e.g. the cathode electrode. As no additional resistive layer is required the fabricating process for such a field emission device is easier, more reliable, and cheaper. In the case of simultaneous use of a multitude of tips, the tip-individual series resistor offers higher tip to tip homogeneity of electron emission, since there is no voltage drop within a group of tips. Furthermore, the "no voltage drop" has the advantage of a lower supply voltage and therefore less power consumption. The less supply voltage also has the advantage to use a more convenient control electronics. Furthermore, it is advantageous from the tip individual series resistor that in the case of a failure, e.g. a short circuit between one tip and its related gate electrode, just this tip fails and all surrounding tips remain unchanged in performance. This offers a high homogeneity and a high overall emission efficiency even in the case of a failure.

The tip is centered in relation to a particularly circular gate aperture that is forming an electrode, the gate electrode. This gate electrode allows advantageously easy and precise emission control. Furthermore, the emission and the acceleration of the emitted electrons can be controlled separately. It is extremely advantageous for the tips to project above the surface of the electrode forming the gate aperture. If the tip apex sticks out of the gate electrode surface level to a defined amount the voltage for a constant current stays constant. Building field emission devices with this kind of geometry offers a large process window at the same

ideal performance. This makes the manufacturing of such devices easier and increases their reliability.

The tip comprises a body of a first material forming the series resistor and a coating of a second material providing for electron emission. This separation of the tip in two components allows more flexibility in view to the optimization of both materials with respect to their objects. Furthermore, a particularly thin coating of the tip body with the relatively expensive electron emission material offers the possibility of cost reduction during the fabrication process.

In an embodiment of the invention a high resistivity material is used for the body of the tip and a material with a low work function is used for the coating of the tip. This is advantageous since the high resistivity material allows the realization of a small tip geometry with significant resistance value. The low work function material is also advantageous since it allows a high emission efficiency already at relatively low voltages.

In a further embodiment of the invention the high resistivity material is an amorphous or polycrystalline silicon, which is no- or low-doped and the low work function material is tungsten (W) or molybdenum (Mo). The use of silicon for the high resistivity material is advantageous, because the resistivity of silicon can be easily modified, either at the time of deposition of the silicon film or after deposition of the silicon film by using diffusion or ion implantation methods. Furthermore, silicon is a very usual material, available in very high purity, relatively low in cost, and can be deposited by various depositing methods. The use of tungsten or molybdenum as a low work function material is advantageous, because those material are very usual for electron emission devices and can be deposited by using standard depositing techniques and equipment.

In a further embodiment of the invention the tip is low-ohmic or directly connected to a first electrode, which is usually the cathode electrode, and which is formed on a substrate.
This is advantageous since it offers a very low or even no voltage drop between the tip and the cathode electrode which leads to a high emission efficiency.

The tip may be opposed to an electrode on a second substrate which comprises also a photon emitting layer, in particular a phosphorous layer. This electrode is used for the acceleration of the emitted electrons and allows easy and precise control for the energy of electrons when arriving at the second substrate. The photo emitting layer allows advantageously the use of field emission devices as light emitting sources.

Field emission devices may be used in the technical field of flat panel displays. Therefore, it is advantageous that field emission devices offer the possibility of realizing light emitting sources with high brightness, high contrast, low power consumption, and easy fabricating processes using standard semiconductor technology leading to a flexible and relatively cheap production method.

The use of a multitude of field emission devices in the field of flat panel displays with a pixel-oriented organization offers the advantage of easy adaption of the flat panel device to applications that require low or high brightness, low or high resolution, low or high contrast, and small or large display size.

The use of a multitude of field emission devices in the field of flat panel displays with a pixel-triple-organization offers the advantage of the possible realization of full color displays.

With the invention related to a method for fabricating a field emission device as described in independent claim 6, the disadvantages previously described for the prior art are eliminated. The fabrication method as disclosed in the present application offers the advantage of relaxed lithographic, etching, and depositing process requirements. Furthermore, this offers a higher flexibility concerning the selection of process technology and is in particular advantageous in view of large-size flat panel displays. It is also advantageous, that the disclosed fabrication method offers the possibility of easy and precise control of the lateral and vertical tip-to-gate distance. Using the relaxed lithographic, etching, and depositing technology requirements the lateral and vertical tip-to-gate distance can be well controlled even in the submicron region. A small lateral tip-to-gate distance offers a high field emission efficiency at lower voltages and less power consumption which is in particular advantageous for battery powered arrangements as flat panel displays for mobile computers. The low supply voltage is furthermore advantageous because it allows a more convenient control electronics. It is a further advantage of the disclosed fabrication method that it provides a complete cathode, electron emission tip, and gate electrode. Furthermore, it is advantageous that the tip height, shape and the amount to which the tip projects above the surface level of the gate electrode can be controlled easily.

The separation in first and second dielectric layer as described in the fabrication method is advantageous for providing a reliable etch stop on the first dielectric layer when etching back the second dielectric layer. The accuracy which is defined by this etch stop defines later on the tip-to-gate electrode distance and the gate opening size which is one of the most important factors for electron emission efficiency and reliability.

1st dielec. etch stop

In a further elaboration of the method for fabrication it is advantageous that the combination of SiO_2- and Si_3N_4-layers offers the possibility of selective etching with a high selectivity and a reliable etch stop. For the use of a polymer as well as for substrates or dielectric layer it is advantageous that the polymer can be removed by laser irradiation or can be dissolved chemically.

In a further elaborated method for fabrication the usage of semiconductor process technology offers high volume production, low cost, high precision and high reliability.

Due to the disclosed method for fabricating electron emission devices the tip height and radius is extremely uniform. The lateral and vertical tip-to-gate electrode

distance can easily be controlled down to submicron dimensions which allows field emission at low supply voltages. This leads to a lower power consumption which is an important fact for battery recharge cycles in portable display systems but allows also the use of a more convenient electronic control circuit. The disclosed method for fabrication allows a high degree of freedom in the choice of the critical materials like tip emitter metal and substrate sizes.

Brief Description of the Drawings

Fig. 1A to Fig. 1F show a preferred embodiment of the invention according to the method for fabricating field emission devices;

Fig. 2A to Fig. 2K show another preferred embodiment of the invention according to a slightly modified method for fabricating field emission devices;

Fig. 3A to Fig. 3E show still another embodiment of the invention according to a modified method for fabricating field emission devices;

Fig. 4A to Fig. 4C show a further embodiment of the invention according to a method slightly modified with regard to the method for fabricating field emission devices of Fig. 3A to Fig. 3E;

Fig. 5A schematically shows a tip projecting above (to an extent +X) or lying below (to an extent -X) the surface of the gate aperture electrode;

Fig. 5B is a diagram showing the voltage for a constant current as a function of X;
(both Figs 5A and 5B are published in Spindt et al. J.Appl.Phys., Vol. 47, No. 12, Dec.1976)

Fig. 6 is a SEM picture of a silicon tip array;

Fig. 7 is a SEM picture of a tip array after the etching back of the second insulator layer;

Fig. 8A and Fig. 8B are SEM pictures of a tip array and a tip after the forming of the gate electrode.

Figs. 1A to 1F show a process sequence as an embodiment of the method for fabricating field emission devices. The semiconductor substrate 7 in Fig. 1A already contains a multitude of tips 1. A preferred material for the substrate 7 is silicon. The tips 1 can be fabricated as shown in Fig. 2B to 2D by masking the substrate with tip masks 8, by creating tips 1 by underetching the tip mask and by subsequently removing the tip masks. A SEM picture of a silicon tip array according to the process level of Fig. 1A is shown in Fig. 6.
As shown in Fig. 1B a first insulating layer 9 is deposited or grown on the surface and coats the total surface of the substrate. The first insulating layer 9 can be thermal SiO_2 or silicon nitride. Now in Fig. 1C a second insulating layer 10 is deposited on the first insulating layer 9. This second insulating layer is used for planarizing the surface of the substrate and is made of a material which allows to planarize an array of tips. Suitable materials are polymers and silicate glass, preferable polyimide or resist materials. Depending on the tip height the thickness of the planarizing layer has to be chosen; in one embodiment with a tip height of about 8 µm the planarizing layer had a thickness of about 10 µm.

In the next step shown in Fig. 1D the second insulating layer 10 is etched back by plasma etching until the tips are projecting above the surface of the second insulating layer.
Fig.7 shows a SEM micrograph of a field emitter array after oxidation of the tips, after coating the tips with polyimide and after the back etch of the polyimide layer.

In Fig. 1E those portions of the first insulating layer 9 which are directly coating the tips are removed by a wet selective etchant. In the case of SiO_2 being the material of the first insulating layer the etchant is HF or buffered HF.

Finally as shown in Fig.1F the substrate is metallized by depositing a metal layer 4 on the upper portion 5 of the tip and on the surface of the second insulating layer 10. The metal layer 4 deposited on the insulating layer 10 forms the gate electrode of the device. The metal layer deposited should be stable and offer a low work function. Preferably gold or Cr/Au is chosen.

The deposition process has to be controlled very carefully to avoid electrical shortening between the tips and the surrounding gate electrode. On the other hand the gap between the tip and the surrounding gate electrode should be as small as possible as this would reduce the threshold voltage for field emission considerably.

The process sequence used here allows to chose the ideal emitter material which appears to be gold since no structuring of the deposited metal layer is required.
Fig. 8A and Fig. 8B show SEM pictures of a tip array and a tip with the finished structure including the gate metal.
The embodiment described above is extremely simple to manufacture and will mainly be used as large area cold electron source in a field emitter device in vacuum applications.

Fig. 2A to Fig. 2K show another preferred embodiment of the invention according to a sligthly modified method for fabricating the field emission devices. This embodiment is well suited for being used in display applications.

In Fig. 2A the substrate 7 which in this case preferably is a glass plate is coated with a conductive layer 13, preferably a metal layer. Layer 13 is structured to form conductive stripes 13 which are the cathode electrodes in the final device.

The fabrication of the tips is shown in Figs. 2B to

2D. First a semiconductor layer 14, preferably a polysilicon layer, is deposited on the conductive stripes. By masking the semiconductor layer with tip masks 8, by underetching the tip masks in a dry or wet etching step and by subsequently removing the tip masks a multitude of tips is formed.

After removal of the tip masks 8 the tips 1 and the cathode electrodes 13 are coated by a first insulating layer 9 and by a second insulating layer 10 as shown in Figs. 2E and 2F. In this embodiment the later step of etching back the second insulating layer 10 to obtain a planarized structure as shown in Figs. 2G and 2H is a chemical-mechanical polishing step.
During this chemical-mechanical polishing step the first insulating layer 9 acts as an etch stop layer. A suitable material for this purpose is Si_3N_4. The chemical-mechanical polishing step is controlled in a way that the nitride layer 9 covering the tips 1 forms an etch stop. This is very important to avoid damage of the tips caused by the etch back step.

Fig. 2I shows the device after the removal of those portions of first insulating layer 9 which were covering the tips. The tips now stick out against the surface of the second insulating layer 10. The final device with a metal layer 4 forming the gate electrode and covering the upper portion of the tips is shown in Fig. 2K.

Both Figs. 1F and 2K clearly emphasize one major performance advantage of the proposed devices in that the tips 1 project above the surface of the surrounding electrode 4 forming the gate aperture 3. Figs. 5A and 5B explain the dependencies between the tip/gate geometries and the current/voltage behaviour as a function of these geometries. Generally a low threshold voltage for the on-set of field emission is advantageous for each device irrespective of its specific application.

For a field emitter display it is however in addition very important that the range of the threshold voltages at which the individual tips emit is as small as possible. This allows for a better multiplexing behaviour. When the tip apex in Fig. 5A is below the surface level of the gate electrode, which corresponds to the left side of the zero line in Fig. 5B, and is moving towards zero, the voltage for a constant current is decreasing. The voltage decreases until the tip apex has reached a lowest level of a few hundred nanometers above the bottom surface of the gate electrode. If the tip apex increases to stick out of the gate elctrode surface level, the voltage stays constant.

Building field emitters with this kind of geometry offers a large process window for the manufacturing process and at the same time excellent performance. All critical dimensions of the tips and the gate electrode like the diameter of the gate aperture, the radius of the tip, the tip angle or the distance between the tip and the gate aperture are independently controllable during the manufacturing process steps. The easy manufacturability and the high multiplexibility due to the narrow threshold voltage distribution allow the extension to large area field emitter devices.

Two further process sequences shown in Figs. 3A to 3E and 4A to 4C offer processes for low cost large area field emitter devices. These devices are also suitable as cold electron emitters in vacuum microelectronic devices or as cathode devices in flat panel displays.

In Fig. 3A the tip masks 8, preferable of SiO_2, have been used to form truncated cones 1 on a silicon substrate by known photolithography and etching steps. A further wet or dry etching step leads to the structure with overhanging tip masks in Fig. 3B. By thermal oxidation the truncated cones are shrinked to provide sharp tips and at the same time to build up the first insulating layer 9 covering the sharp tips and the surface of the substrate. As to be seen in Fig. 3C the overhanging tip masks have not been removed during or after the thermal oxidation step.

Next a metal layer 4 is deposited, preferably by evaporating a metal that closely sticks to the underlying insulating layer 9 and that allows to transport a small gate current. The metal layer covers the insulating layer 9 as well as the overhanging tip masks as to be seen in Fig. 3D. Suitable is a chromium/gold deposition.

In Fig. 3E the tip masks 8 with the metal coating thereon and those portions of the insulating layer 9 which directly cover the top part of the tips are removed. This may be done by etching with buffered HF. On the backside of the substrate one or more conductive layers 11, 12 may be provided which are used as series resistance or allow better contacting of the substrate.

Fig. 4A corresponds to the substrate 7 with sharpened tips 1 covered by the insulating layer 9 of Fig. 3C. In Fig. 4B a second insulating layer 10 is deposited and etched back to a defined level. A suitable material for this layer is photo resist or polyimide, materials which may be applied by spin coating. It is important that the overhanging tip masks are sticking out of the surface of the etched back insulating layer 10.

The further steps necessary to complete the device as shown in Fig. 4C correspond to the steps already described in Figs.3D and 3E.

In the slightly modified device of Fig. 4C the gate electrode 4 is parallel to the surface of the substrate. The dielectric portion formed by the first and second insulating layers 9, 10 is much thicker thus offering a much lower device capacity.
This kind of device is therefore especially suitable for some high frequency circuits.

Claims

1. A field emission device comprising a tip (1) for emitting electrons,
said tip (1) having a body (2) of a first material, said body (2) forming a series resistor,
wherein said tip (1) is centered in relation to a gate aperture (3), in particular a circular gate aperture, said gate aperture (3) being formed by an electrode (4),
characterised in that

said tip (1) projects above the surface of said electrode (4) forming the gate aperture (3).

2. The field emission device of claim 1 wherein said tip (1) further comprises an at least partial coating (5) of a second material, said coating providing for electron emission.

3. The field emission device of claim 1 or 2 wherein said first material is a material with high resistivity, said first material comprising no- or low-doped amorphous or polycrystalline silicon.

4. The field emission device of claim 2 wherein said second material is a material with low work function, preferably W or Mo.

5. The field emission device of any of the preceding claims 1 to 4 wherein said tip (1) with said series resistor is low-ohmic coupled, in particular directly connected, to an electrode (6) formed as a conductive layer on a substrate (7).

6. A method for fabricating a field emission device, said method comprising the steps of:

   a) providing a semiconductor substrate (7),

   b) masking said substrate (7) with tip masks (8),

   c) creating tips (1) by underetching said tip masks (8),

   d) removing said tip masks (8),

   e) coating the total surface of said substrate (7) with a first insulating layer (9),

   f) depositing a second insulating layer (10) on said first insulating layer (9),

   g) etching back said second insulating layer (10) until said tips (1) are projecting above the surface of said second insulating layer (10),

   h) removing those portions of said first insulating layer (9) directly coating said tips (1) and

   i) metallizing said substrate (7) thus forming a gate electrode (4).

7. The method according to claim 6 wherein

   - step c) and step e) are combined to one process step, said process step including shrinking said tips (1) by thermal oxidation to provide sharp tips thus coating the total surface of said substrate (7) with said first insulating layer (9),

   - step d) is not carried out,

   - step i) is carried out before step h) with step i) including metallizing said tip masks (8) and

   - step h) is removing those portions of said first insulating layer (9) directly coating the top part of said tips (1) and includes removing of said tip masks (8).

8. The method according to claim 7 wherein steps f) and g) are not carried out.

9. The method according to claim 7 or 8 wherein step a) or step i) include providing a conducting layer (11, 12) on the backside of said substrate (7).

10. The method according to claim 6 wherein

   - step a) includes coating said substrate (7) with a conductive layer (13), structuring said conductive layer to form conductive stripes (13) and depositing a semiconductor layer (14) on said conductive stripes (13) and

   - step b) is masking said semiconductor layer (14) with said tip masks (8).

11. The method according to any of the preceding claims 6 to 10 wherein
said first insulating layer (9) is a SiO_2-layer or a Si_3N_4-layer,
said second insulating layer (10) is a polymer like polyimide, a resist or a silicate glass,
said etching back said second insulating layer (10) uses a plasma etch step,
said partially removing said first insulating layer (9) uses a wet etch step and
the material used for metallizing said substrate is stable and offers a low work function as for example Au or Cr/Au.

12. The method according to claim 6 wherein
said first insulating layer (9) is a Si_3N_4-layer,
said second insulating layer (10) is SiO_2,
said etching back said second insulating layer (10) uses a chemical-mechanical polishing step,
said partially removing said first insulating layer (9) uses a wet etch step and
the material used for metallizing said substrate is stable and offers a low work function as for example Au or Cr/Au.

13. The method according to any of the preceding claims 6 to 12 wherein
all said masking, etching, removing, coating, depositing, structuring and metallizing steps are

performed with semiconductor process technology.

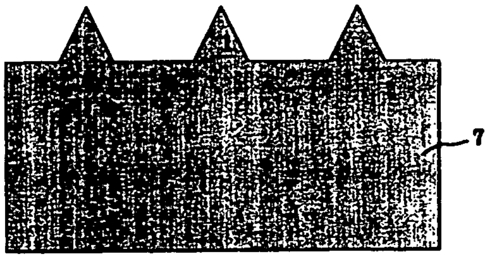

FIG. 1A

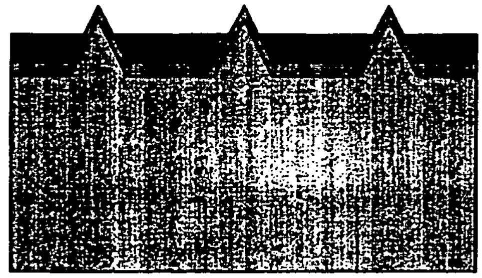

FIG. 1D

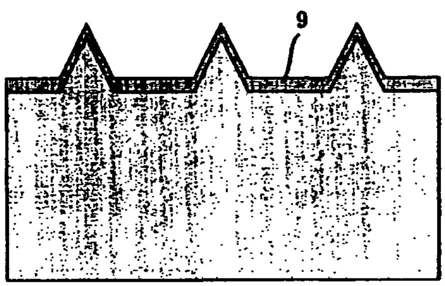

FIG. 1B

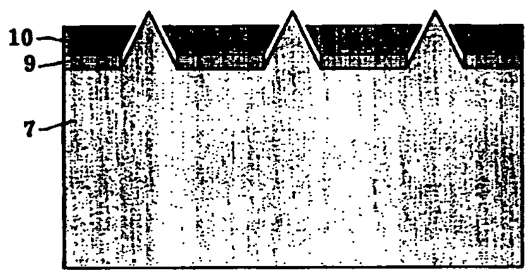

FIG. 1E

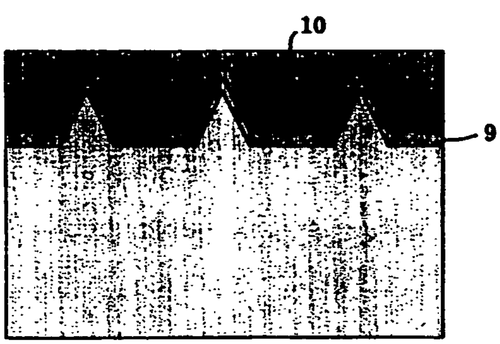

FIG. 1C

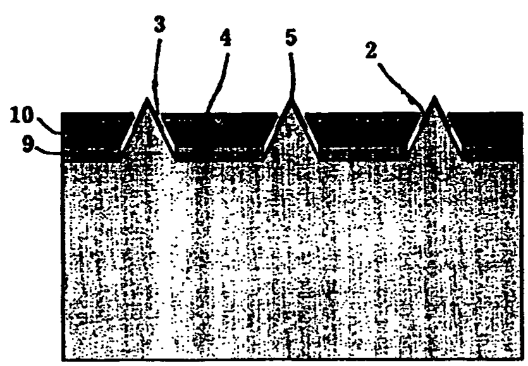

FIG. 1F

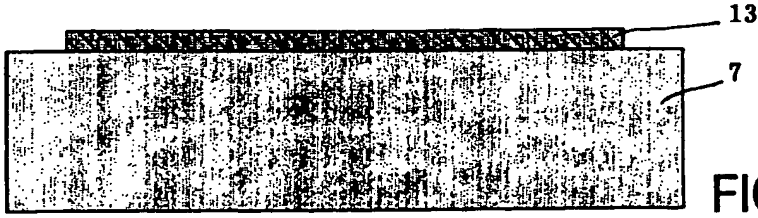

FIG. 2A

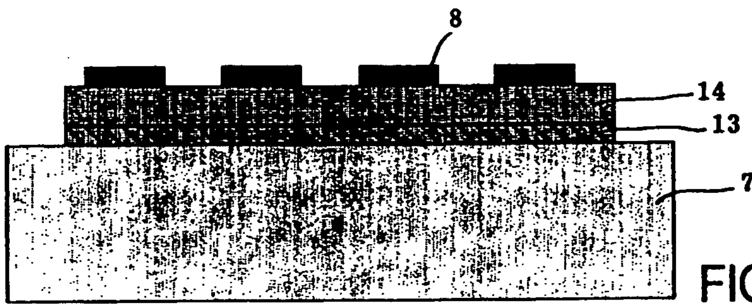

FIG. 2B

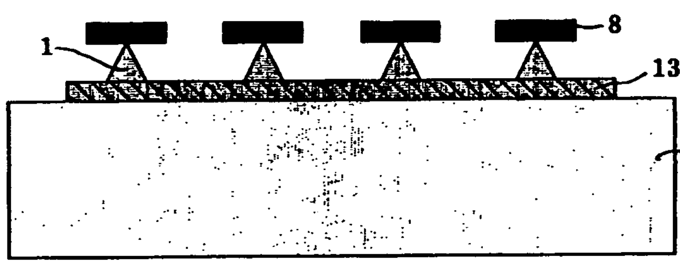

FIG. 2C

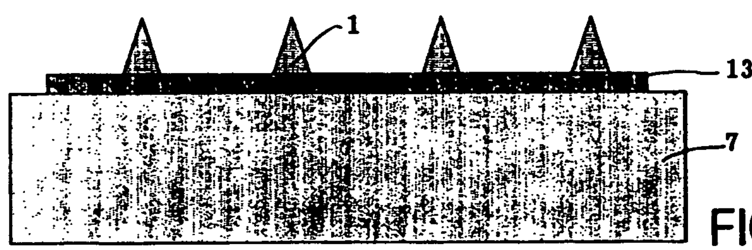

FIG. 2D

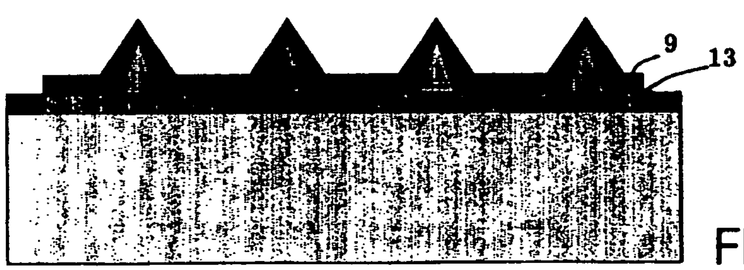

FIG. 2E

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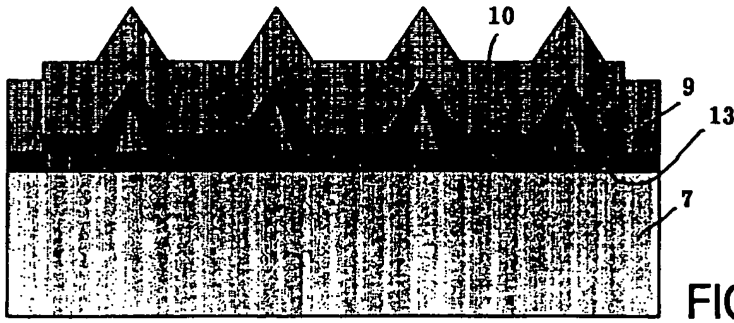

FIG. 2F

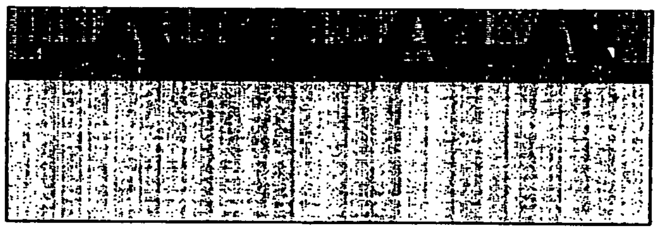

FIG. 2G

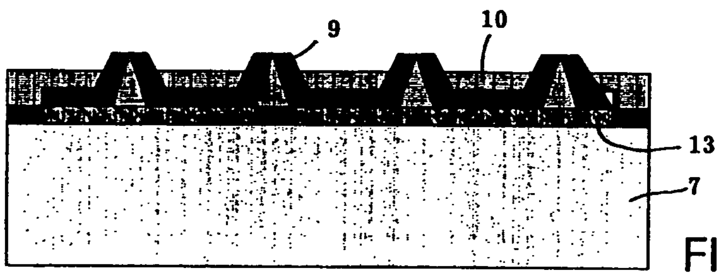

FIG. 2H

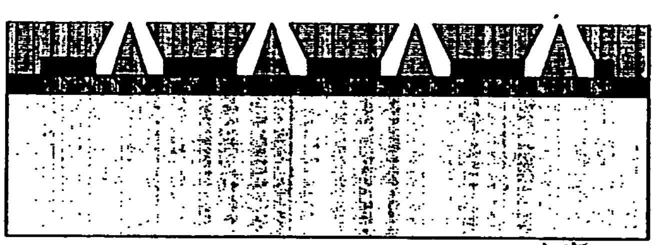

FIG. 2I

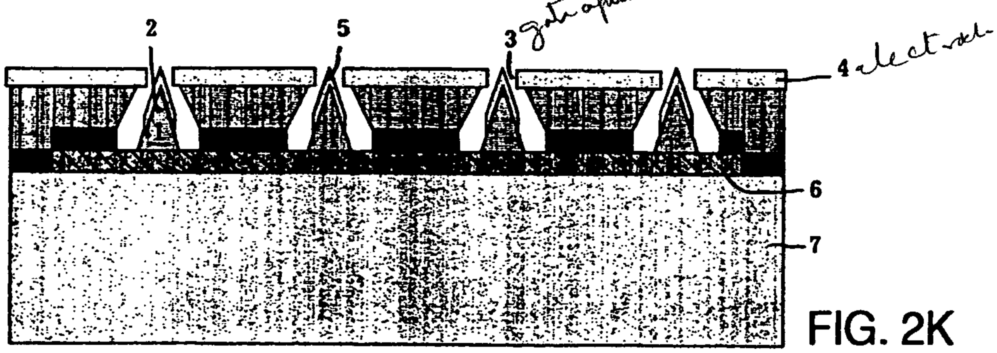

FIG. 2K

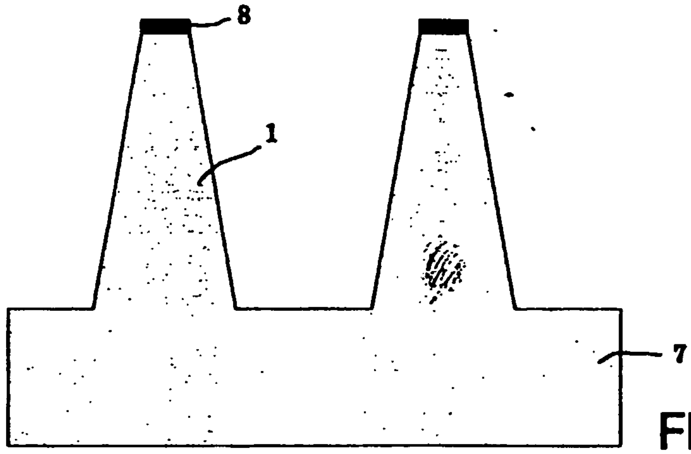

FIG. 3A

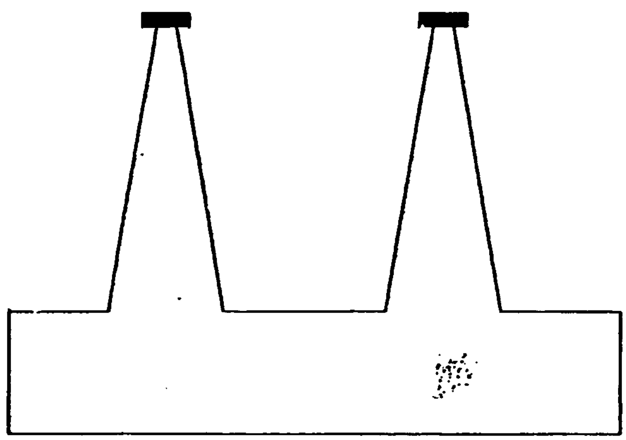

FIG. 3B

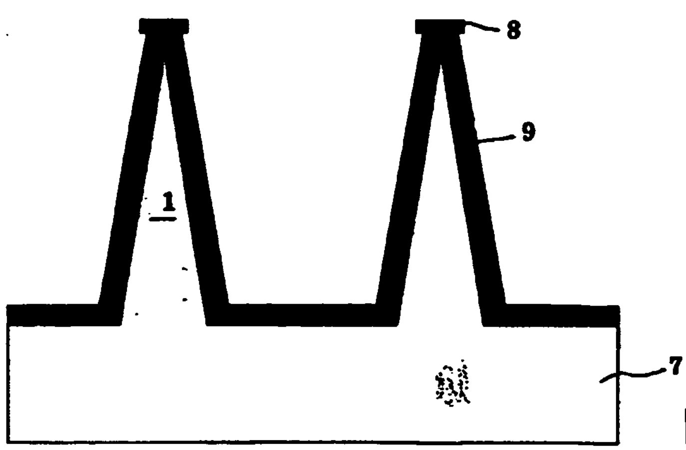

FIG. 3C

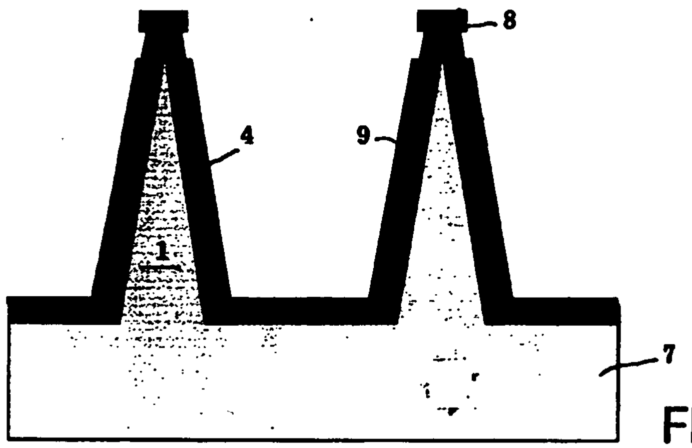

FIG. 3D

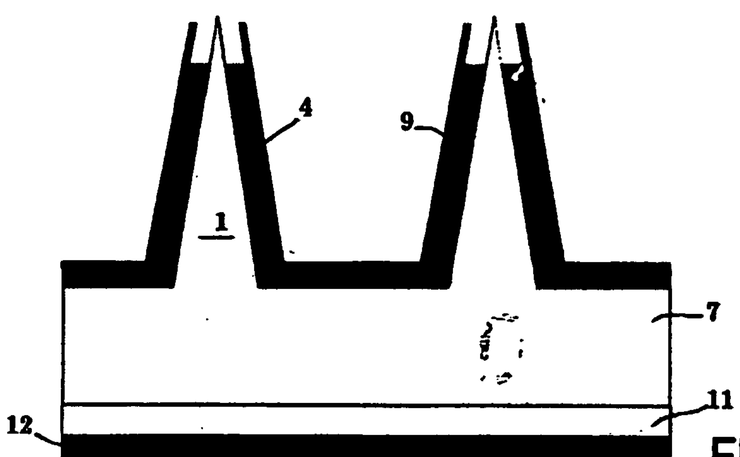

FIG. 3E

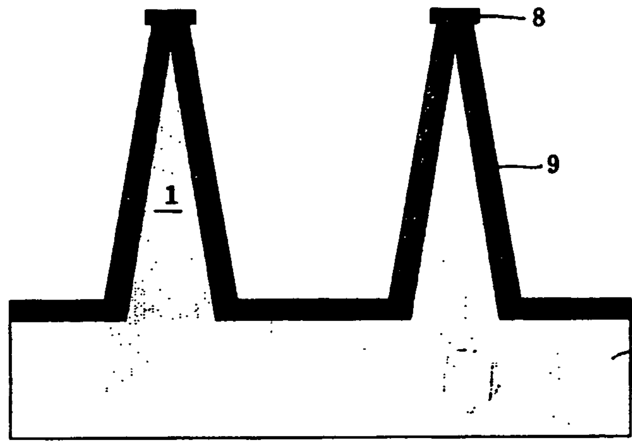

FIG. 4A

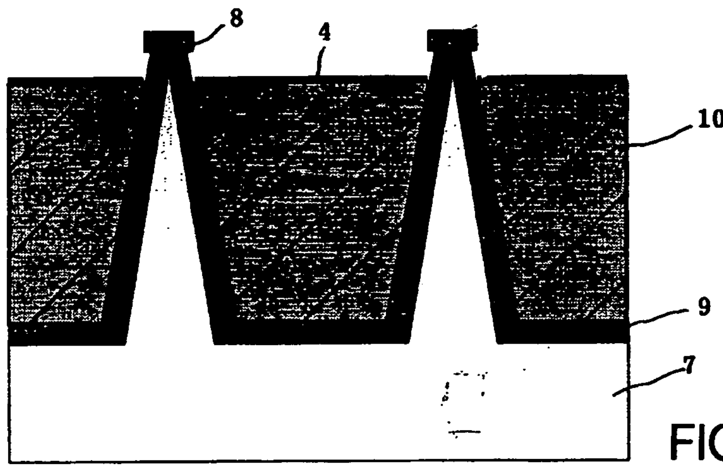

FIG. 4B

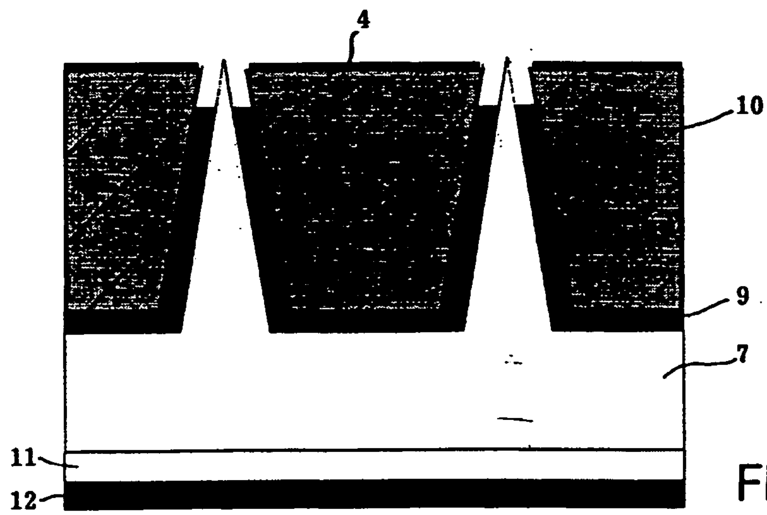

FIG. 4C

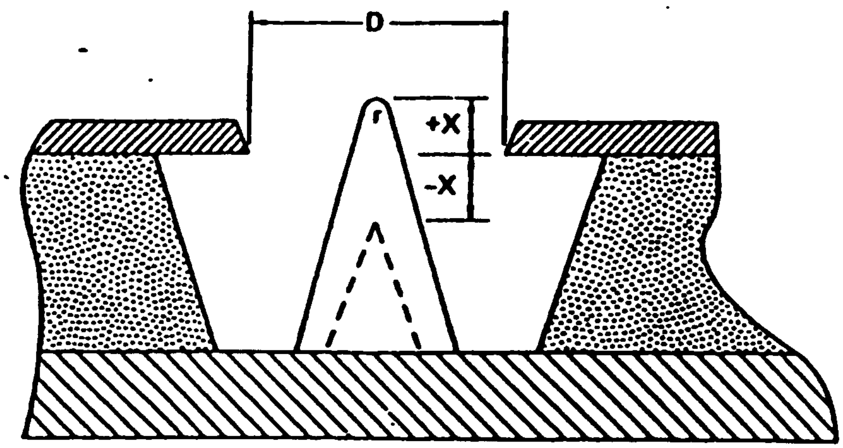

FIG. 5A Effect of changes of cathode dimensions in the 100-cone array. (Dimensions in μm.)

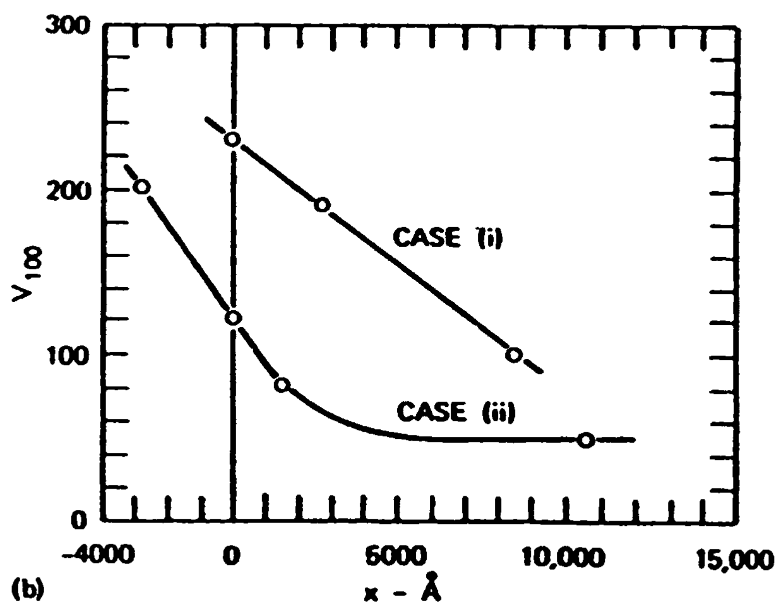

FIG. 5B Voltage for 100 μA as a function of x. Case (i) $r = 600$ Å, $D = 1.9$ μm; case (ii) $r = 500$ Å, $D = 1.3$ μm.

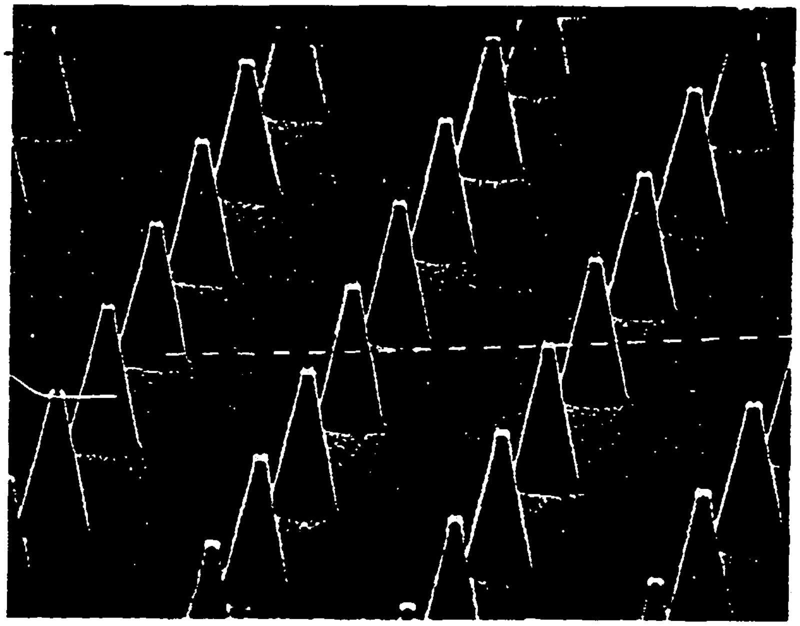

FIG. 6

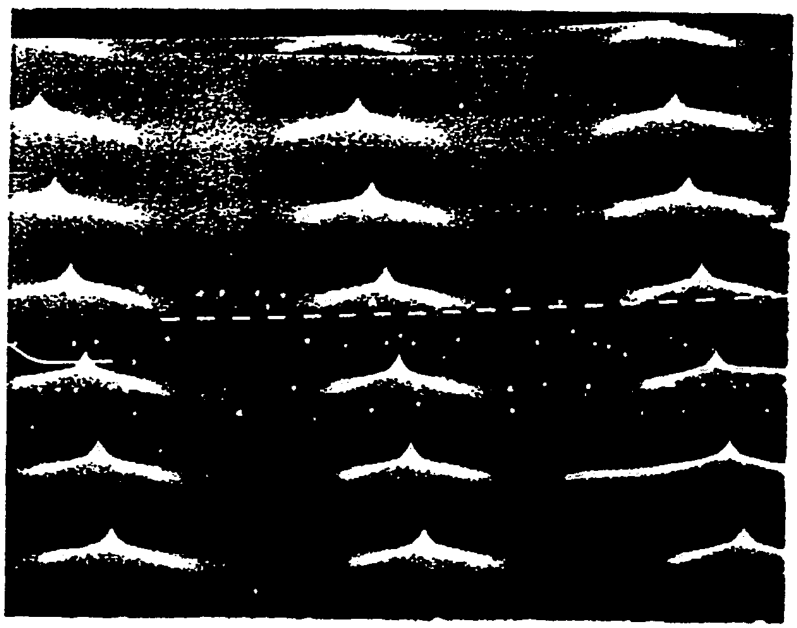

FIG. 7

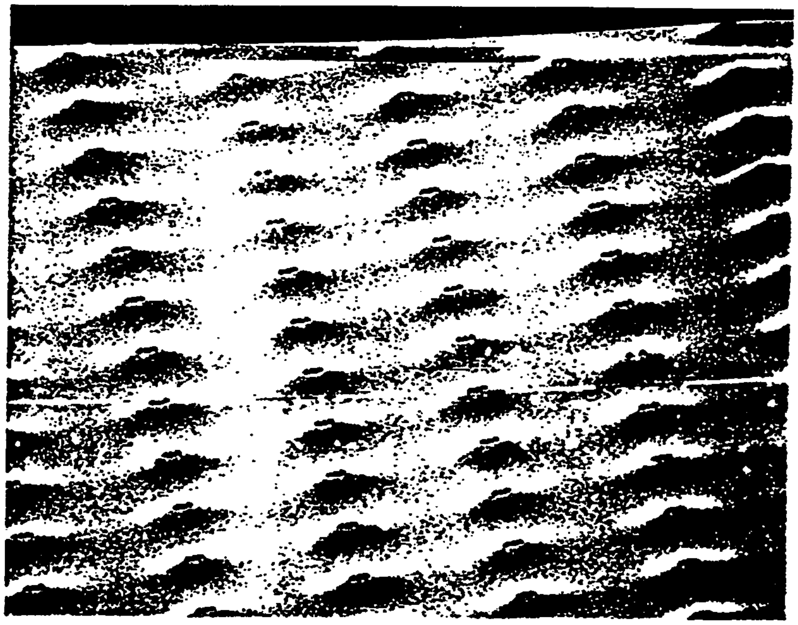

FIG. 8A

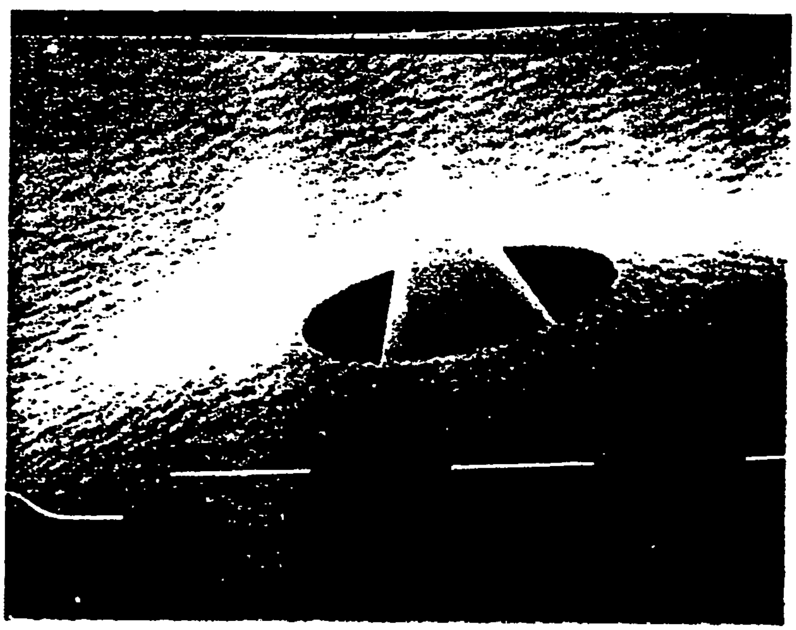

FIG. 8B

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EUROPEAN SEARCH REPORT

Application Number
EP 96 10 1877

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	FR-A-2 650 119 (THOMSON TUBES ELECTRONIQUES) 25 January 1991 * page 2, line 19 - line 32 * * page 5, line 11 - line 17 * * page 6, line 6 - line 15 * * claims 1-9 * * figure 2 * ---	1-5	H01J1/30 H01J3/02
Y	JOURNAL OF MICROMECHANICS & MICROENGINEERING, vol. 2, 1 January 1992, pages 43-74, XP000560006 BUSTA H H: "VACUUM MICROELECTRONICS 1992" * page 52, left-hand column, paragraph 3 - right-hand column * * page 54, right-hand column, paragraph 1 * * page 55, left-hand column, paragraph 3 - page 56, right-hand column, paragraph 1 * * figures 24-31 * ---	1-5	
X	FR-A-2 700 222 (SAMSUNG DISPLAY DEVICES CO LTD) 8 July 1994 * figures 4A-4H * * page 5, line 17 - page 8, line 10 * ---	6	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01J
E	WO-A-96 04674 (CENTRAL RESEARCH LAB LTD ;ALLEN PHILIP CHARLES (GB)) 15 February 1996 * figures 12-15 * * page 7, line 23 - page 8, line 20 * --- -/--	8	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 July 1996	Colvin, G

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EUROPEAN SEARCH REPORT

Application Number
EP 96 10 1877

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	JOURNAL OF APPLIED PHYSICS, vol. 47, no. 12, 1 December 1976, pages 5248-5263, XP000560520 SPINDT C A ET AL: "PHYSICAL PROPERTIES OF THIN-FILM FIELD EMISSION CATHODES WITH MOLYBDENUM CONES" * page 5254, left-hand column, paragraph 2 - right-hand column, paragraph 2 * * figure 10 *	1	
A	US-A-5 451 830 (HUANG JAMMY C) 19 September 1995 * figures * * column 2, line 1 - line 4 * * column 2, line 41 - line 43 * * column 2, line 52 - line 57 * * column 3, line 30 - column 4, line 46 * * column 5, line 1 - line 12 * * column 6, line 3 - line 24 *	1-6	
A	US-A-5 394 006 (LIU DAVID N-C) 28 February 1995 * figures 9-13 * * column 4, line 16 - column 6, line 17 *	6	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
D,A	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 38, no. 10, 1 October 1991, pages 2320-2322, XP000225960 GHIS A ET AL: "SEALED VACCUM DEVICES: FLUORESCENT MICROTIP DISPLAYS"	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 July 1996	Colvin, G

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